

GENERATING MULTI-PHASE CLOCK SIGNALS  
USING HIERARCHICAL DELAYS

Abstract of the Disclosure

[0035] Circuits and methods for generating multi-  
5 phase clock signals using digitally-controlled  
hierarchical delay units (HDs) are provided. A  
plurality of serially-coupled HDs outputs clock signals  
that are phase-shifted relative to a reference clock  
signal. Each HD includes either one or two variable  
10 delay lines that provide coarse phase adjustment of an  
associated input signal. Each HD also includes one or  
more phase mixers that provide fine phase adjustment of  
the input signal.